



LCD Module Technical Specification

First Edition
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Final Revision

T-51380L050J-FW-P-AA

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Revision History

Rev.	Date	Page	Comment

1. Application

This technical specification applies to 5" color TFT-LCD module. The applications of the panel are car TV, portable DVD and GPS.

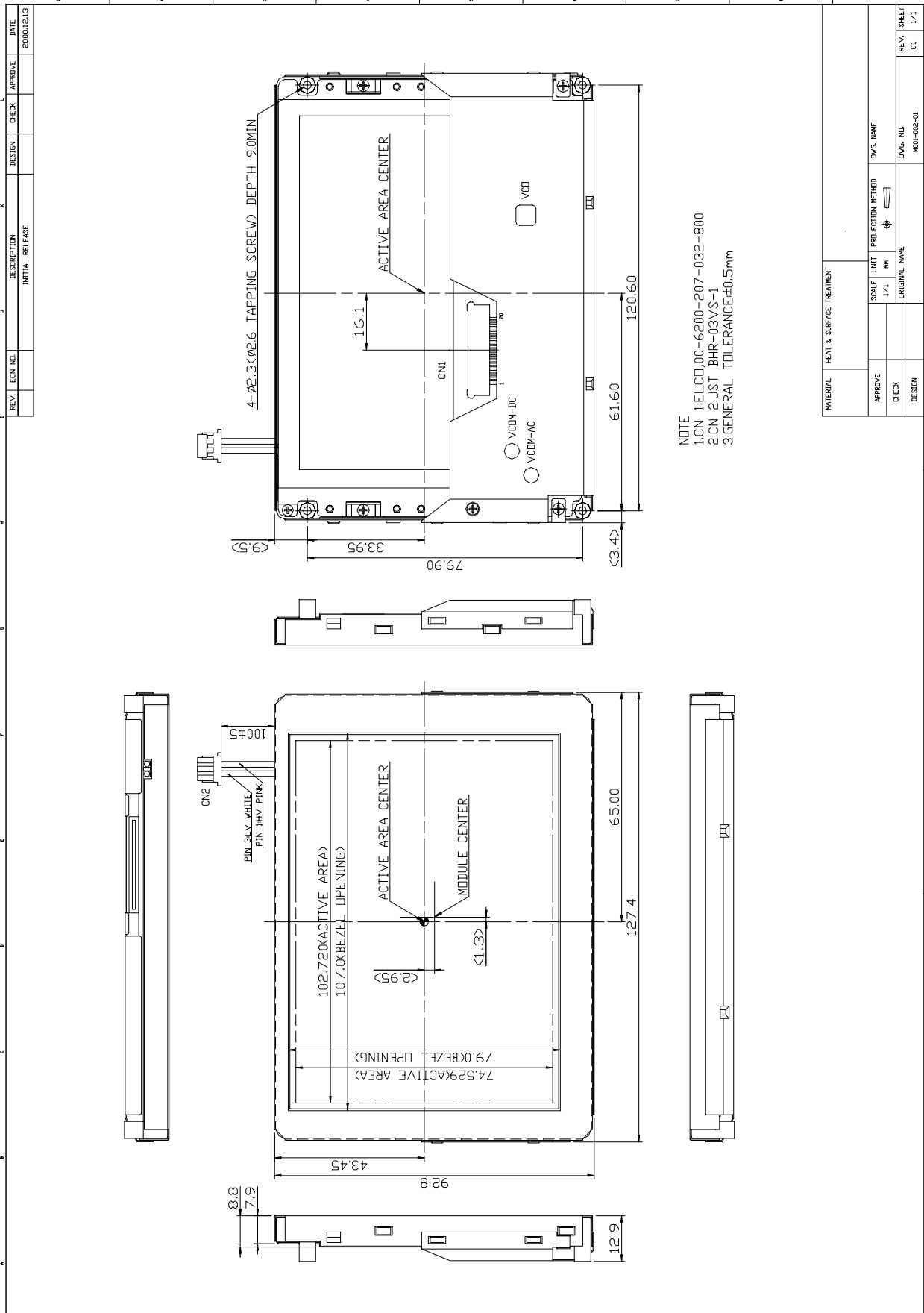
2. Features

- . Compatible with NTSC & PAL system
- . Pixel in stripe configuration
- . Slim and compact
- . Vcom Toggle
- . Image Reversion : Up/Down and Left/Right

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	5 (diagonal)	inch
Display Format	960 × 234	dot
Active Area	102.72 (H) × 74.53 (V)	mm
Dot Pitch	0.107 (H) × 0.319 (V)	mm
Pixel Configuration	Stripe	
Outline Dimension	127.4 (W)×92.8 (H)×12.9 (D)(typ.)	mm
Weight	160±10	g

4. Mechanical Drawing of TFT-LCD Module



REV.	ECN NO.	DESCRIPTION	DESIGN	CHECK	APPROVE	DATE
		INITIAL RELEASE				2000.12.13

MATERIAL		HEAT & SURFACE TREATMENT		DWG. NAME	
APPROVE	SCALE	UNIT	PROJECTION METHOD		
CHECK	1/1	mm	1st		
DESIGN	ORIGINAL NAME		DWG. NO.		
			MOD-002-01		
			REV. SHEET		
			01		
			1/1		

5. Input / Output Terminals

5-1) TFT-LCD Panel Driving

Pin No	Symbol	I/O	Description	Remark
1	$\overline{\text{HSY}}$	I/O	Horizontal Sync. Input / Output	Note 5-1
2	FRP	O	Video Polarity Alternating Signal	
3	CSY	I	Composite Sync. Signal	Note 5-1
4	V _{GH}	I	Supply Voltage for Gate Driver (Hi level)	Note 5-2
5	V _{GL}	I	Supply Voltage for Gate Driver (Low level)	Note 5-3
6	V _B	I	Video Signal (Blue)	
7	V _R	I	Video Signal (Red)	
8	V _G	I	Video Signal (Green)	
9	GND	I	Ground	
10	V _{DD}	I	Supply voltage for Controller	Note 5-4
11	V _{CC}	I	Supply voltage for source driver	Note 5-5
12	GND	I	Ground	
13	CKC	I	Control pin for select I/O signal	Note 5-1
14	$\overline{\text{VSY}}$	I/O	Vertical Sync. Input/ Output	Note 5-1
15	PSI	O	Synchronize Pulse for Decoder	
16	PSC	O	Synchronize Pulse for DC-DC Converter	
17	NC	-	No Connection	
18	UD	I	UP/DOWN Control	Note 5-7
19	RL	I	Right/Left Shift Control	Note 5-6
20	NP	I	NTSC/PAL Input	Note 5-8

Note 5-1 : Pin 13 (CKC) can select the function for Pin 1 ($\overline{\text{HSY}}$), Pin 3 (CSY), and Pin 14 ($\overline{\text{VSY}}$).

Pin 13 (CKC)	Pin 1 ($\overline{\text{HSY}}$)	Pin 3 (CSY)	Pin 14 ($\overline{\text{VSY}}$)
Hi	$\overline{\text{HSY}}$ Output	CSY Input	$\overline{\text{VSY}}$ Output
Low	External Horizontal Sync Input	External Clock Input	External Vertical Sync Input

Note 5-1-1: CKC= High:

- If CKC=1, the phase lock loop (PLL) is adopted in the LCD module.
- Inputs CSY, the controller of LCD module will separate the Vertical Sync and Horizontal Sync from CSY.
- Output Horizontal Sync ($\overline{\text{HSY}}$, Pin 1) and Vertical Sync ($\overline{\text{VSY}}$, Pin 14).
- The internal detect will detect Vertical Sync to reset the vertical counter.

Note 5-1-2: CKC= Low <VGA mode>

- a. If CKC=0, the phase lock loop (PLL) is not adopted in the LCD module.
- b. If CKC=0, the external clock input frequency of Pin 3 is 25.17 MHz.
- c. Input external Vertical Sync (VSY, Pin 14) and Horizontal Sync (Pin 1) to synchronize the LCD module. External Horizontal Sync and External Vertical Sync input pulse can be high going or low going.
- d. The pulse width of external Horizontal Sync input is $4.7\mu s \pm 2\mu s$. The pulse width of external Vertical Sync input is 2H~4H.

Note 5-1-3: If there is any question about CKC=0, please contact PVI.

Note 5-2 : V_{GH} TYP. = +17V

Note 5-3 : V_{GL} TYP. = -15V

Note 5-4 : V_{DD} :+5V

Note 5-5 : V_{CC} TYP. = +5V

Note 5-6 : Hi (+5V) for shift Right; Input Low (0V) for inverse (shift Left).

Note 5-7 : Hi (+5V) for DOWN; Low (0V) for UP.

Note 5-8 : NTSC= Hi(+5V),PAL=Low(0V)

5-2) Backlight driving

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	Wire color : pink
3	VL2	Input terminal (Low voltage side)	Wire color : white Note 5-9

Note 5-9 : Low voltage side of backlight inverter connects with Ground of inverter circuits.

5-3) Input / Output Connector (ELCO,00-6200-207-032-800)

A) LCD Module Connector

FFC Down Connector

20 Pins

Pitch : 1.0 mm

B) Backlight Connector

JST BHR-03VS-1

Pin No. : 3

Pitch : 4 mm

Pink : High Voltage

White : Low Voltage

6. Absolute Maximum Ratings:

GND = 0 V , Ta = 25

Parameter	Symbol	MIN.	MAX.	Unit	Remark	
Supply Voltage For Source Driver	V _{CC}	-0.5	7	V		
	V _{DD}	-0.5	7	V		
Supply Voltage For Gate Driver	V _{GH} - V _{GL}	-0.3	40	V		
	H Level	V _{GH}	0	40	V	
	L Level	V _{GL}	-20	0	V	
Analog Signal Input Level	V _R ,V _G ,V _B	-0.3	7.0	V		
Digital Input Signals		-0.3	5.5	V	Note 6-1	
Digital Output Signals		-0.3	5.5	V	Note 6-2	
Storage Temperature		-30	+80			
Operation Temperature		-20	+70			

Note 6-1 : $\overline{\text{HSY}}$, $\overline{\text{CSY}}$, $\overline{\text{VSY}}$, $\overline{\text{CKC}}$,

Note 6-2 : $\overline{\text{HSY}}$, $\overline{\text{VSY}}$, $\overline{\text{PSI}}$, $\overline{\text{PSC}}$

7. Electrical Characteristics

7-1) Recommended Operating Conditions:

A) Driving for TFT-LCD Panel

GND = 0V , Ta = 25

Parameter	Symbol	MIN.	Typ	MAX	Unit	Remark
Supply Voltage For Source Driver	Analog	V _{CC}	4.5	5.0	5.5	V
	Logic	V _{DD}	4.5	5.0	5.5	V
Supply Voltage For Gate Driver	H level	V _{GH}	+15	+17	+19	V
	L level	V _{GL}	-16	-15	-14	V
Supply Voltage For controller	V _{DD}	4.5	5.0	5.5	V	
Analog Signal input Level	Amplitu	0.3		V _{CC} -0.3	V	
Digital input voltage	H level	V _{IH}	0.7 V _{DD}	-	V _{DD}	V
	L level	V _{IL}	-0.3	-	0.3 V _{DD}	V
Digital output voltage	H level	V _{OH}	0.7 V _{DD}	-	V _{DD}	V
	L level	V _{OL}	-0.3	-	0.3 V _{DD}	V

B) Driving for backlight

Ta= 25

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V_L	387	430	473	Vrms	$I_L = 6 \text{ mA}$
Lamp current	I_L	5.5	6	6.5	mA	
Lamp frequency	P_L	40	43	80	KHz	Note 7-1
Kick-off voltage(25)	V_s	---	---	345	Vrms	Note 7-2
Kick-off voltage(0)	V_s	---	---	520	Vrms	Note 7-2

Note 7-1 : The wave form of lamp driving voltage should be as closed to a perfect SIN wave as possible.

Note 7-2 : The Kick-off times 1sec

7-2) Power Consumption

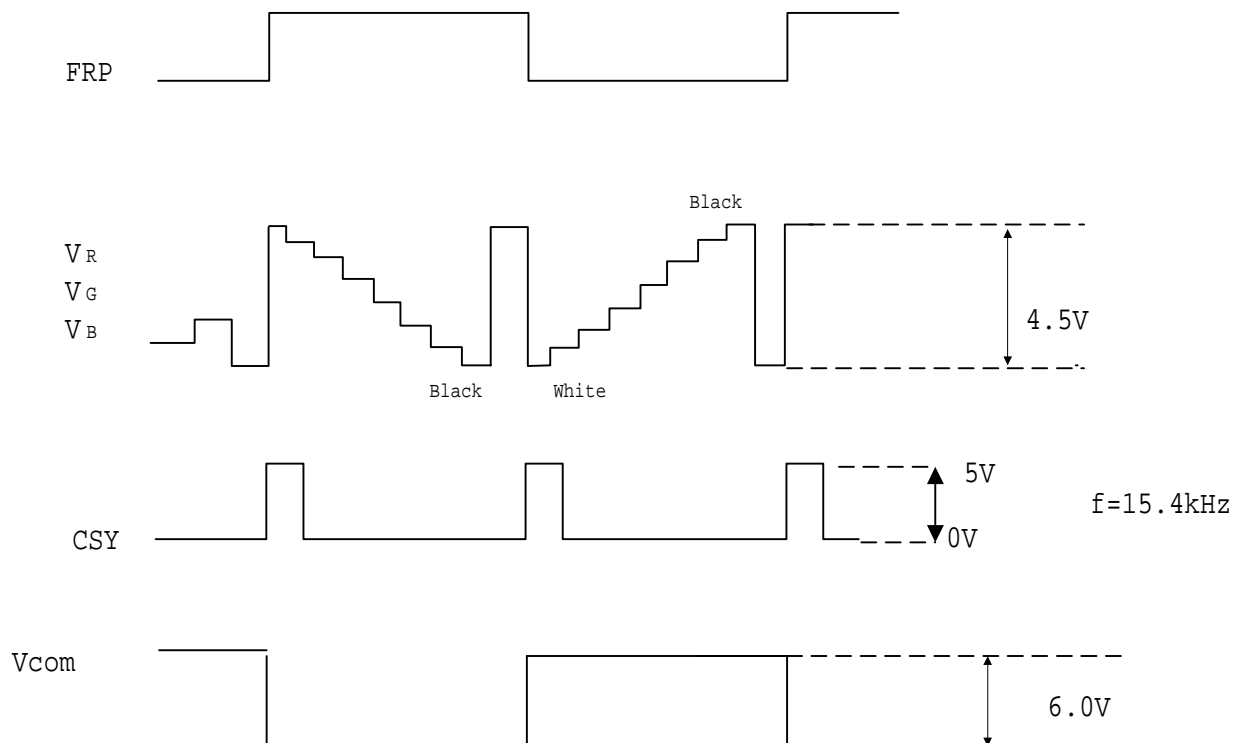
Ta= 25

Parameter	Symbol	Conditions	TYP.	MAX	Unit	Remark
Supply current for Gate Driver (Hi level)	I_{GH}	$V_{GH} = +17V$	0.08	0.1	mA	
Supply current for Gate Driver (Low level)	I_{GL}	$V_{GL} = -15V$	-14.57	-18.94	mA	
Supply current for Source Driver	I_{CC}	$V_{CC} = +5V$	30.95	40.24	mA	
Supply current for controller	I_{DD}	$V_{DD} = +5V$	1.08	1.4	mA	
LCD Panel Power Consumption			0.38	0.49	W	Note 7-3
Backlight Lamp Power Consumption			2.58	3.07	W	Note 7-4

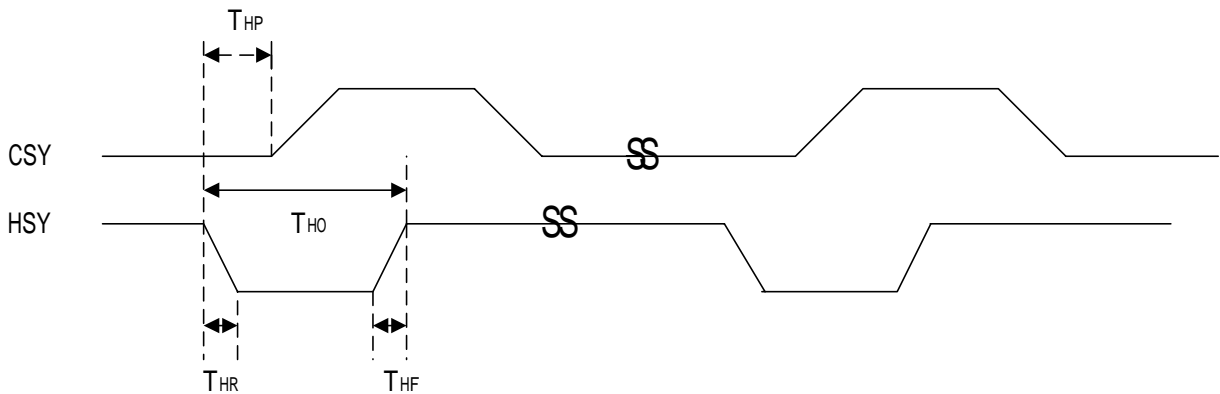
Note 7-3 : The power consumption for backlight is not included.

Note 7-4 : Backlight lamp power consumption is calculated by $I_L \times V_L$.

7-3) Input / Output signal timing chart



Parameter			Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Horizontal Sync. Output	Frequency	NTSC	$F_{HO(N)}$	-	15.73	-	KHz	
		PAL	$F_{HO(P)}$	-	15.63	-	KHz	
Pulse	Pulse Width		T_{HO}	4.4	4.7	5.0	μs	
	Phase Difference		T_{HP}	0	2	-	μs	
	Rising Time		T_{HR}	-	-	0.05	μs	
	Falling Time		T_{HF}	-	-	0.05	μs	
Vertical Sync. Output Pulse	Frequency	NTSC			fh/262.5			
		PAL			fh/312.5			
	Pulse Width		T_{VO}	-	4H	-	μs	
	Phase Difference	NTSC	$T_{VPO(N)}$	-	2H	-	μs	odd field
		PAL	$T_{VPO(P)}$	-	1H	-		
	Phase Difference	NTSC	$T_{VPE(N)}$	-	1.5H	-	μs	even field
		PAL	$T_{VPE(P)}$	-	0.5H	-		



7-4) Display Time Range

A) When sync. Signal of NTSC system is applied.

a) Horizontally

11.35 ~ 61.36 μs .

b) Vertical

22 ~ 252 H

B) When sync. Signal of PAL system is applied.

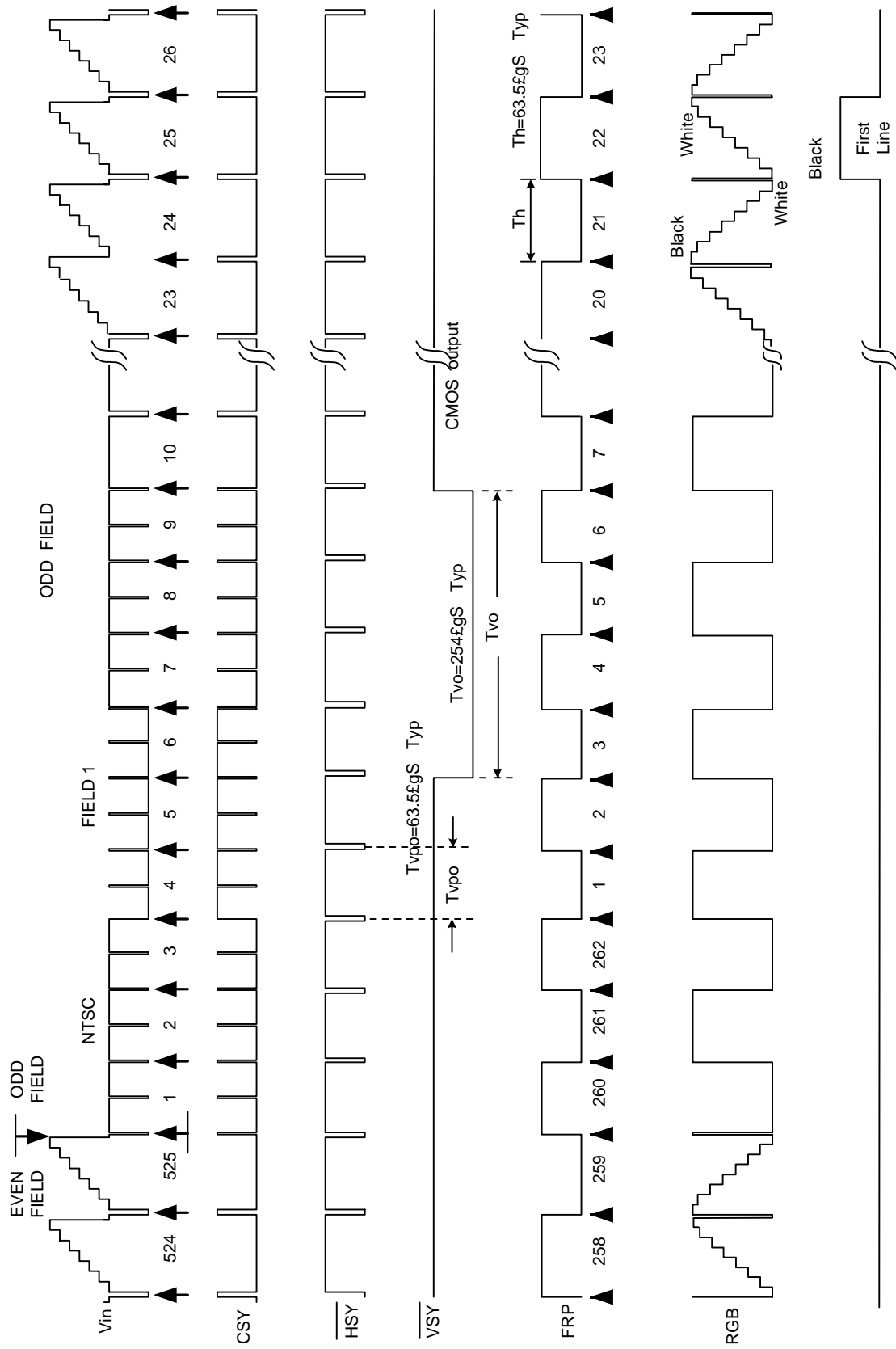
a) Horizontally

11.54 ~ 61.9 μs .

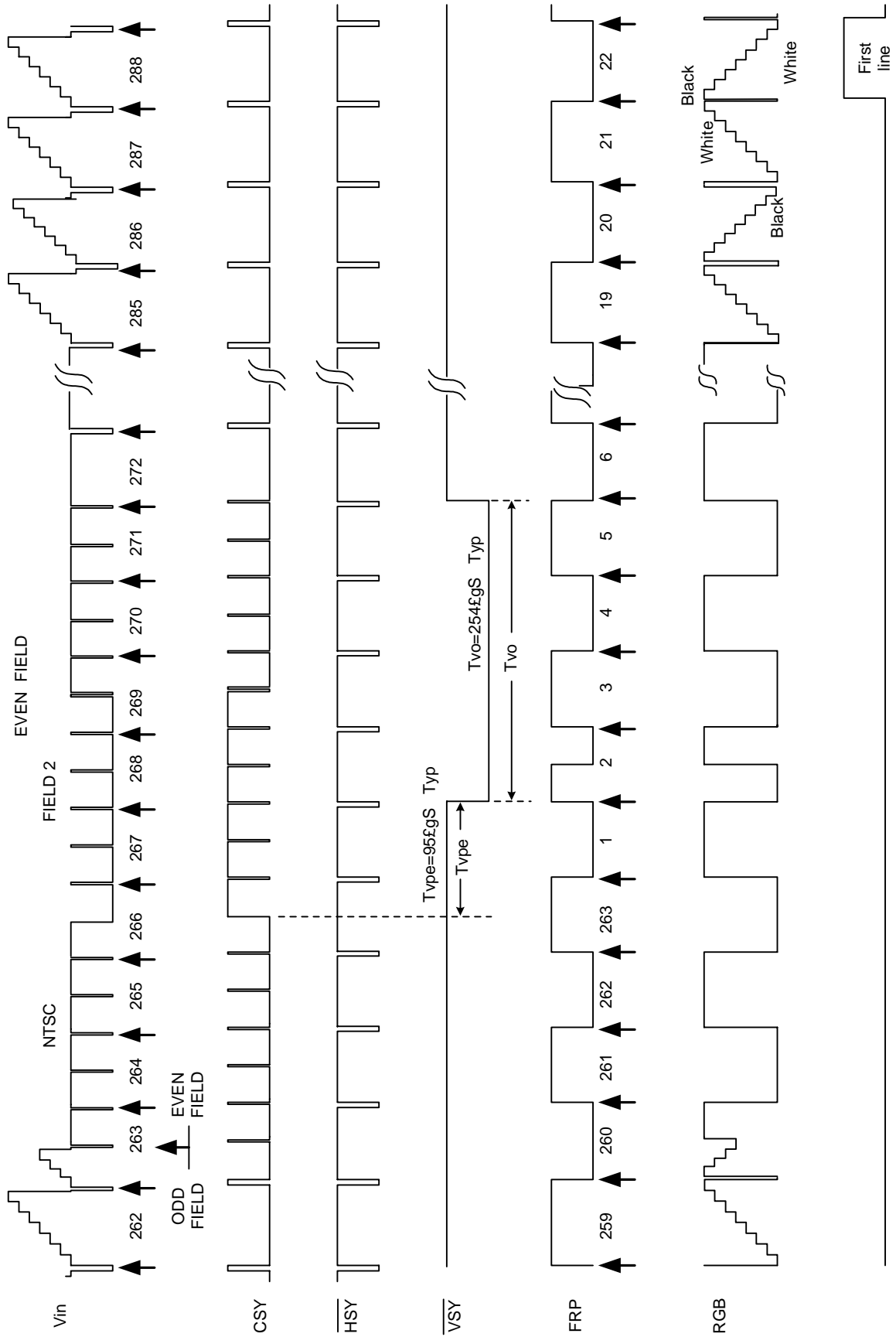
b) Vertical

28 ~ 300 H

C) NTSC System

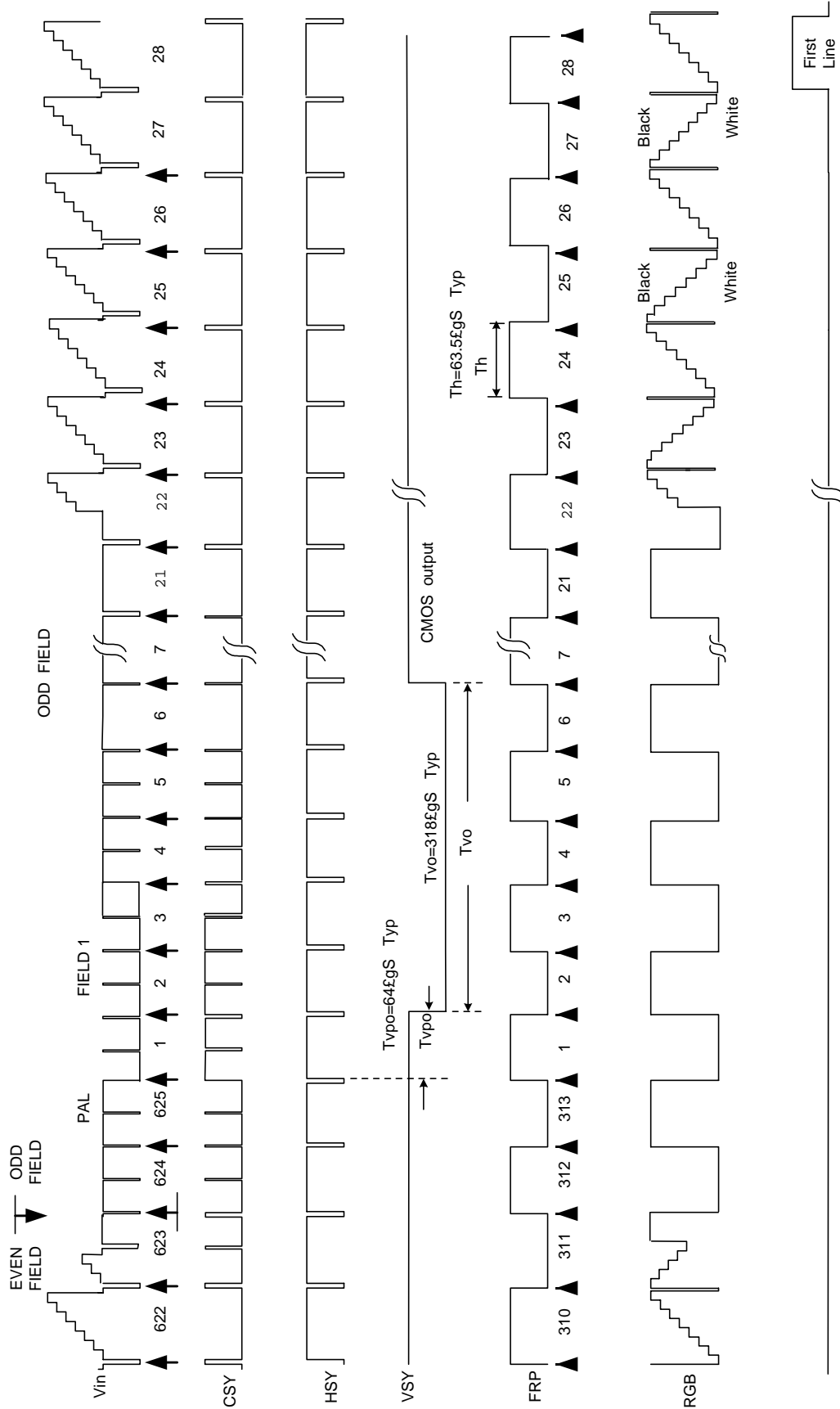


Timing chart of I/O and RGB signal

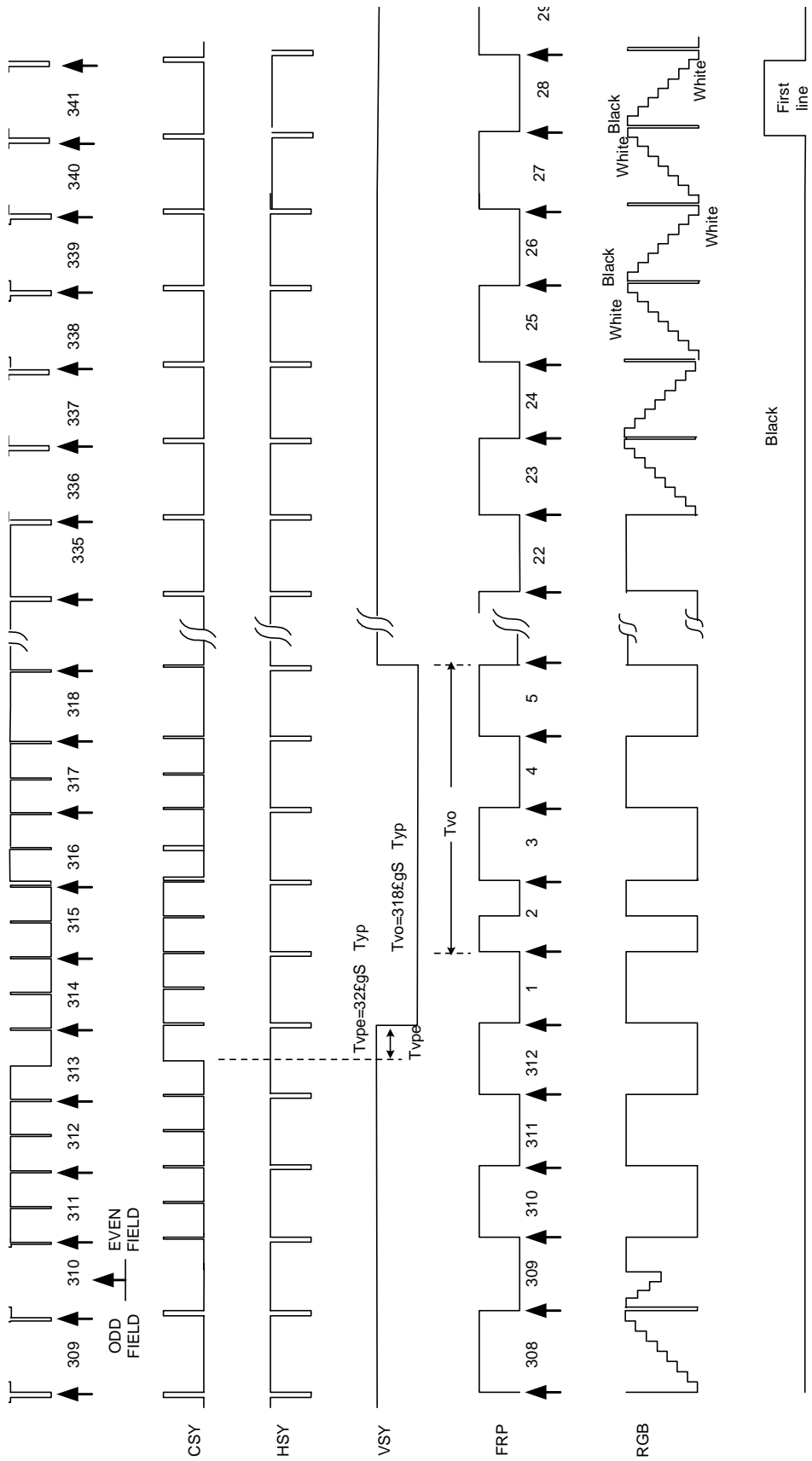


Timing chart of I/O and RGB signal

D) PAL System



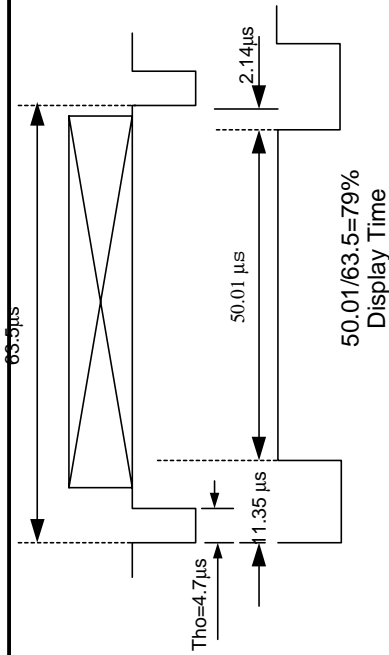
Timing chart of I/O and RGB signal



Timing chart of I/O and RGB signal

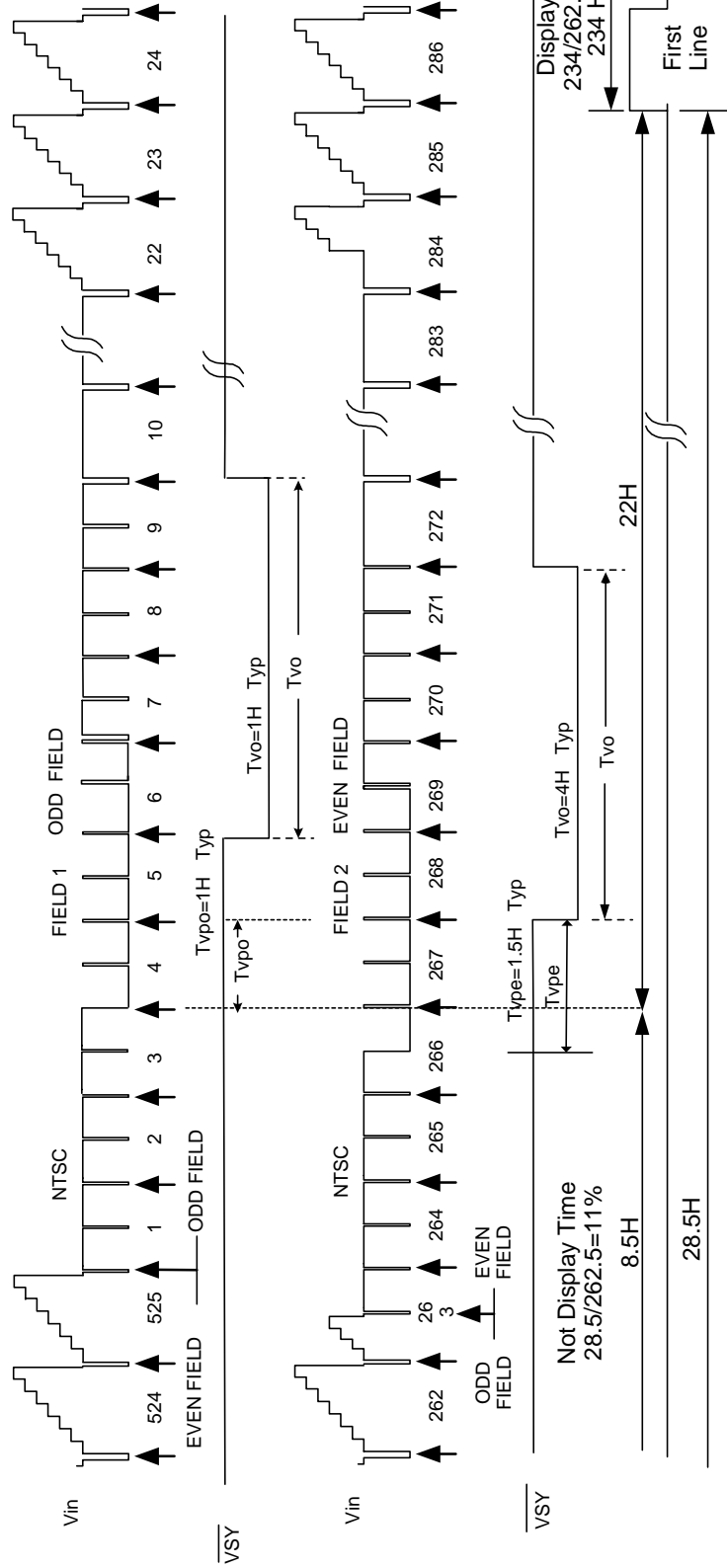
E) Display Timing FOR NTSC & PAL

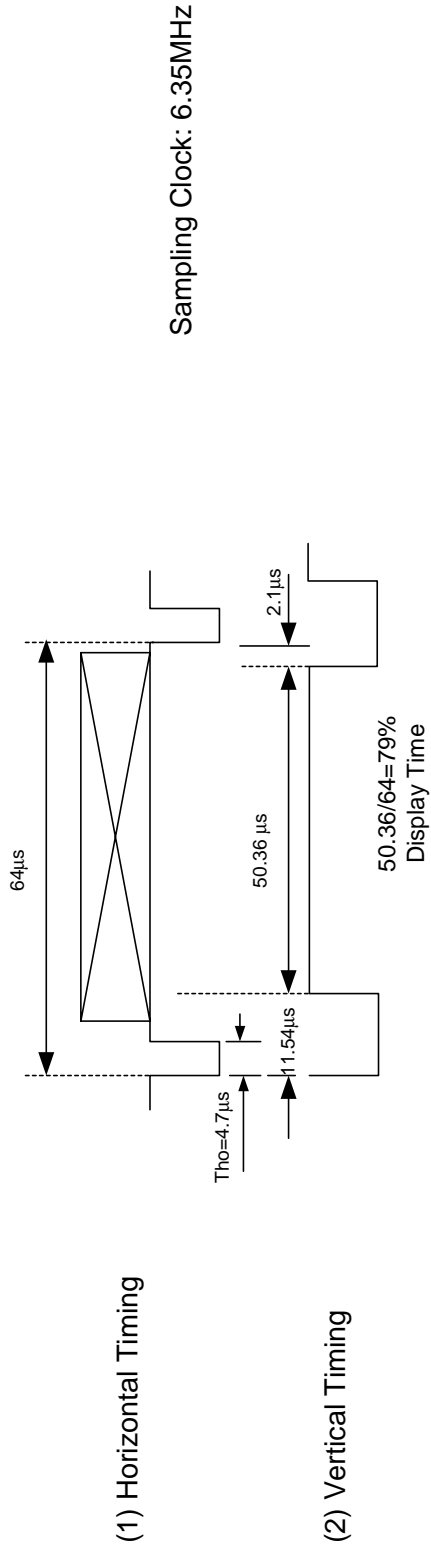
(1) Horizontal Timing Sampling Clock: 6.4MHz



(2) Vertical Timing

50.01/63.5=79%
Display Time





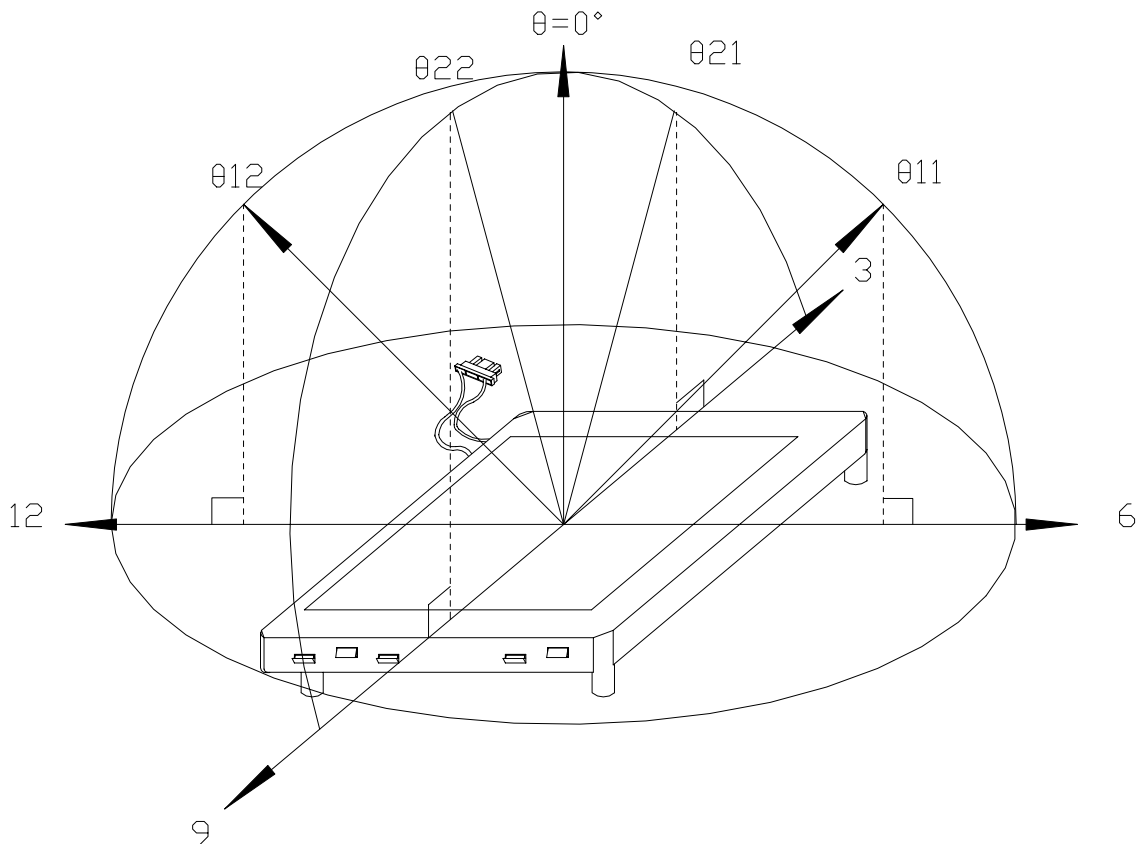
8. Optical Characteristics

8-1) Specification:

Ta = 25

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	21, 22	CR 10	45	55		deg	Note 8-1
	Vertical	11		10	15		deg	Note 8-1
		12		30	35		deg	Note 8-1
Contrast Ratio		CR	=0°	80	150			Note 8-2
Response time	Rise	Tr	=0°			30	ms	Note 8-4
	Fall	Tf				50	ms	
Brightness				300	350		cd/m ²	Note 8-3
White Chromaticity		x	=0°	0.250	0.300	0.350		Note 8-3
		y	=0°	0.300	0.350	0.400		
Lamp Life Time +25				10,000			hr	

Note 8-1: The definitions of viewing angles



Note 8-2 : $CR = \frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

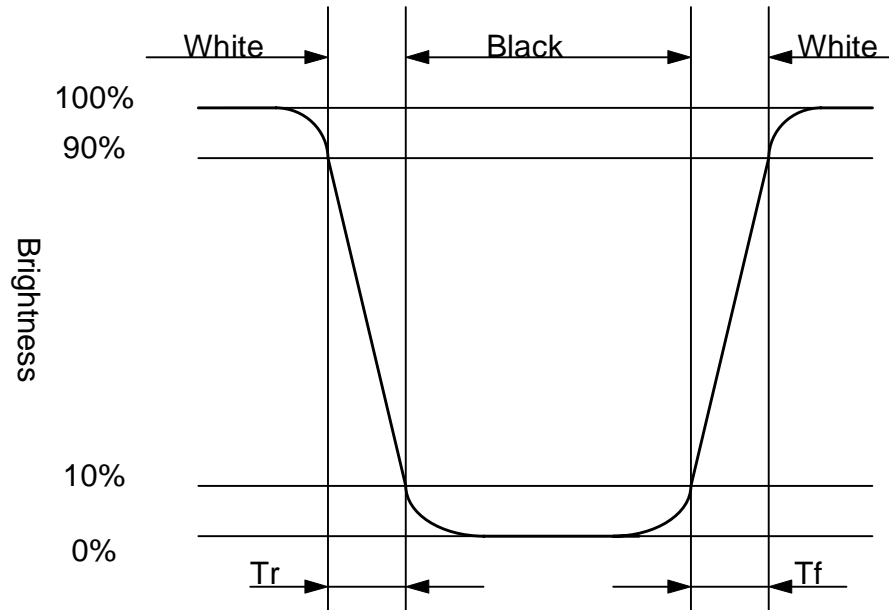
(Testing configuration see 8-2)

Contrast Ratio is measured in optimum common electrode voltage.

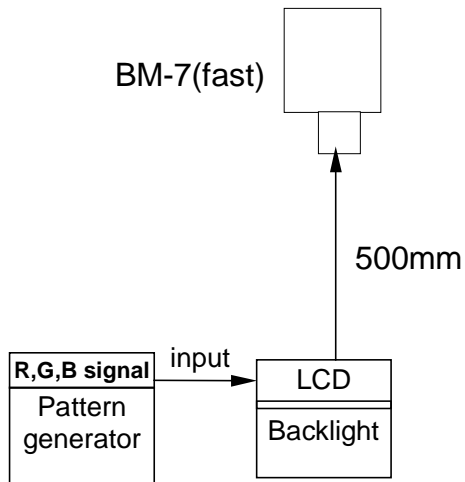
Note 8-3 : Topcon BM-7(fast) luminance meter 2 ° field of view is used in the testing (after 20~30 minutes operation).

Lamp Current 6mA

Note 8-4: The definition of response time:

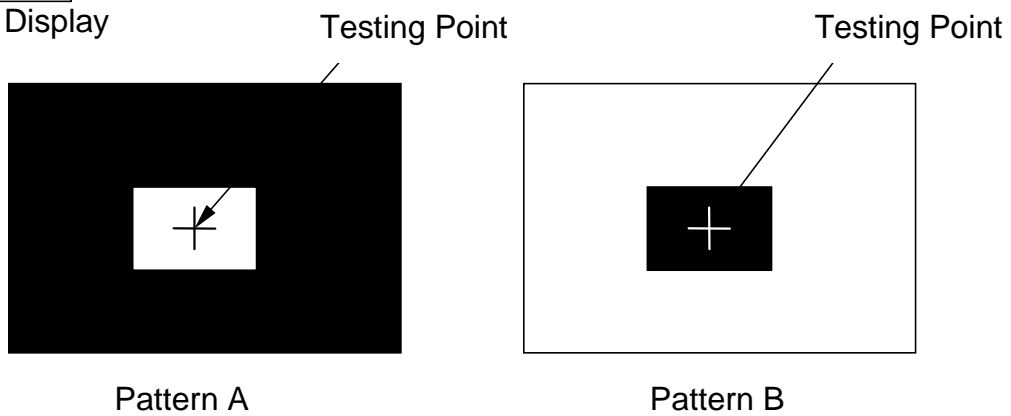


8-2) Testing configuration

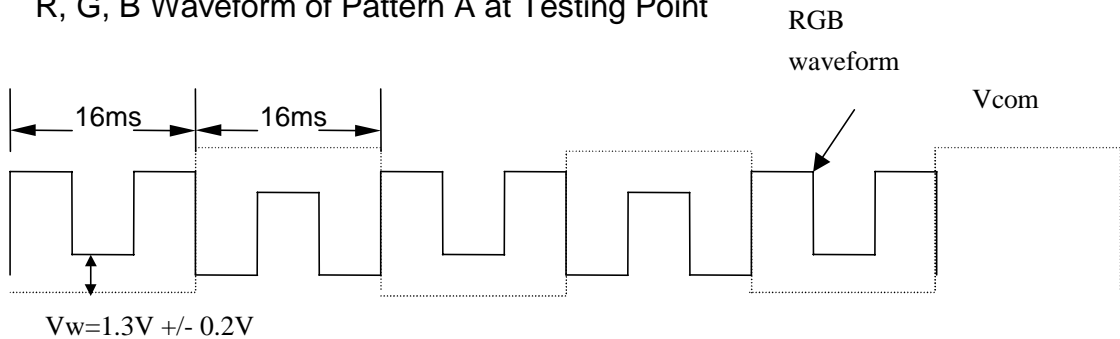


Caution: 1. Environmental illumination 1 lux
 2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

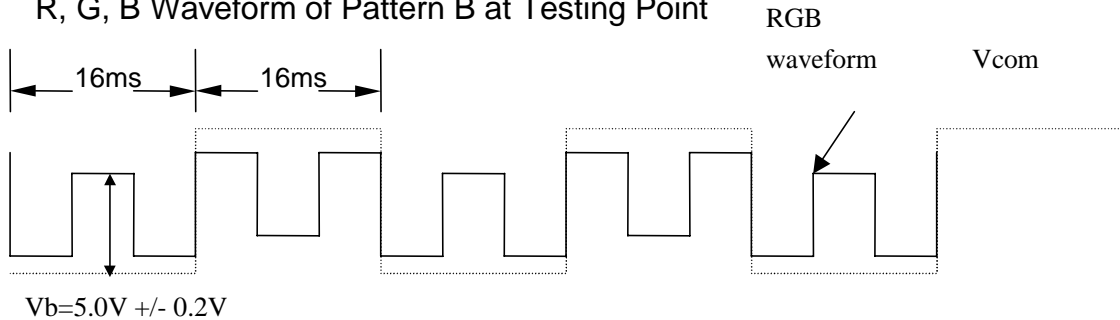
- LCD Display



- R, G, B Waveform of Pattern A at Testing Point



- R, G, B Waveform of Pattern B at Testing Point



9. Handling Cautions

9-1) Mounting of module

- a) Please power off the module when you connect the input/output connector.
- b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.
 - 1. The noise from the backlight unit will increase.
 - 2. The output from inverter circuit will be unstable.
 - 3. In some cases a part of module will heat.
- c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

9-2) Precautions in mounting

- a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
- b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

9-3) Adjusting module

- a) Adjusting volumes on the rear face of the module have been set optimally before shipment.
- b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

9-4) Others

- a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- b) Store the module at a room temperature place.
- c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- d) If LCD panel breaks, it is possible that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- e) Observe all other precautionary requirements in handling general electronic components.
- f) Please adjust the voltage of common electrode as material of attachment by 1 module.

10. Reliability Test

No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +80 , 240 hrs
2	Low Temperature Storage Test	Ta = -30 , 240 hrs
3	High Temperature Operation Test	Ta = +70 , 240 hrs
4	Low Temperature Operation Test	Ta = -20 , 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = +60 , 95%RH, 240 hrs
6	Thermal Cycling Test (non-operating)	-25 +25 +70 , 200 Cycles 30 min 5min 30 min
7	Vibration Test (non-operating)	Frequency : 10 ~ 55 Hz Amplitude : 1.5 mm Sweep time: 11 mins Test Period: 6 Cycles for each direction of X, Y, Z
8	Shock Test (non-operating)	100G, 6ms Direction: ± X, ± Y, ± Z Cycle: 3 times
9	Electrostatic Discharge Test (non-operating)	150pF, 330 Air: ±15KV; Contact: ±8KV 10 times/point, 5 points/panel face

Ta: ambient temperature

[Criteria]

Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

11. Block Diagram

